



White paper

# DSP based multi standard analog TV demodulator

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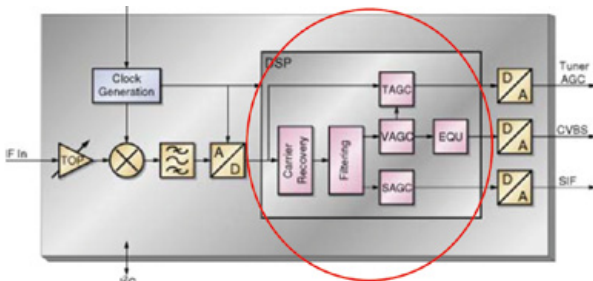
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## Customer

The customer is a world known international company playing significant role in various fields of TV consumer electronic market. Their product portfolio comprises of numerous analog and digital TV audio and video integrated circuits.

## Project Overview

The goal of the project was a development of SystemC model and its simulation environment, as well as FPGA prototyping environment for next generation of the DSP based multi standard analog TV demodulator. Both developed environments were used for several purposes: as concept verification environment, as pre-silicon SW development environment, as pre-silicon demonstration platform and development environment for new and/or improved algorithms. All of this helped on efficient solving of long design cycle in the presence of shorter Time-to-Market pressures for product with increasingly shorter market windows.



*DSP based analog TV demodulator  
(FPGA design architecture circled)*

The initial project concept was developed in a joint action with concept, HW and SW design engineers. Critical points in design were identified in order to provide optimal SystemC model and FPGA design.

Demodulator SystemC model was designed as synthesizable from the scratch, in order to be used as a HDL description for FPGA prototyping. Synopsis CoCentric System Studio SW was used as design and simulation environment for demodulator SystemC model.

After successful verification phase, demodulator SystemC model was converted to Verilog model using Synopsys SystemC Compiler SW. Functional co-verification of these two models was done using Cadence Incisive simulation SW. Verilog model was used as input to the FPGA prototyping phase.

Field Programmable Gate Array (FPGA) technology, powered with advanced simulation and synthesis tools is becoming the most preferred platform for the rapid prototyping of integrated digital systems. Due to its nature, FPGA internally is capable to support prototyping of pure digital designs, but it also provides connectivity to real (usually analog) world.

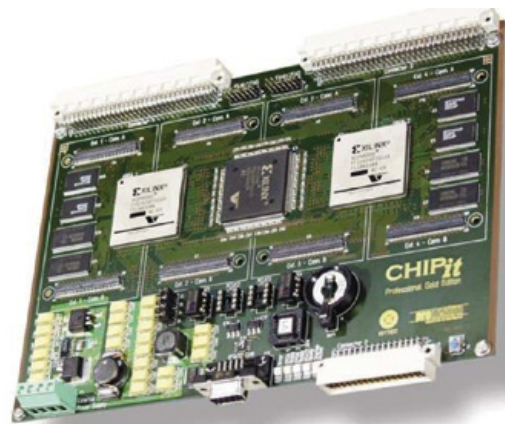
Main challenge during FPGA development was design of FPGA specific workarounds for ASIC specific RTL modules (internal memories, PLLs, clocks, ...)

FPGA development process comprised of two major parts:

- Functional verification of FPGA RTL code
- Synthesis of FPGA RTL code for specific prototyping platform

Functional verification of FPGA RTL was done using same SW tool environment as for functional co-verification from the previous phase.

Synthesis was performed with Synplicity Certify, ProDesign Chipit Manager and Xilinx XST SW, all for prototyping platform ProDesign CHIPit Gold.



*Photo of prototyping platform*

The developed prototyping environment is able to provide "near ASIC" functionality, easy DSP and micro controller SW development and RTL code debugging, as well as versatile interfaces. Interfaces on extension board provide window from FPGA digital design into multiple analog video and audio (ADC, DACs), communication (I2C) and peripheral world (LEDs, switches and push-buttons).

The development lasted four months. It involved two SystemC/FPGA design engineers and one engineer for DSP and micro controller software support for SystemC simulation and FPGA design bring up, as well as one project manager.

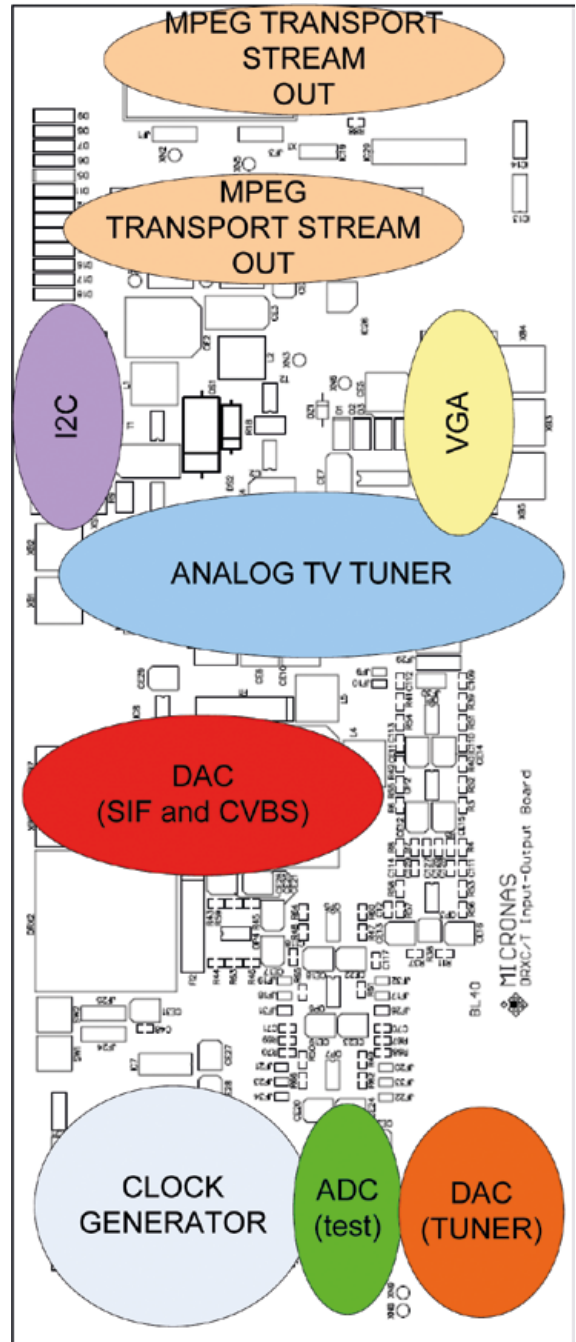
**Benefits**

The project covered the complete development from the prototyping environment idea until HW/SW prototyping platform. All development steps were either conducted or organized by RT-RK, in correspondence with the customer. The final solution fulfills the customer requirements in terms of performances. The complete development process and costs were transparent to the customer via regular meetings and appropriate reports.

**Prototyping Environment Gallery**



*Photo of prototyping environment for DSP based analog TV demodulator IC*



*Extension board PCB sections*

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