RT - RK
COMPUTER BASED SYSTEMS

White paper

Highly complex integrated circuit for Digital TV

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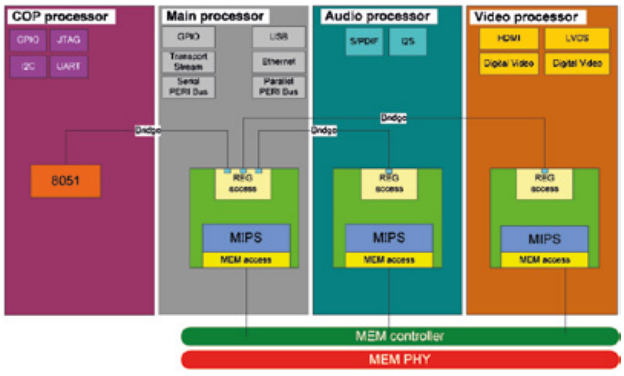
Customer

The customer is a world known international company playing significant role in various fields of TV consumer electronic market. Their product portfolio comprises of numerous analog and digital TV audio and video integrated circuits.

Project Overview

The goal of the project was a development of prototyping environment for next generation of highly complex digital TV integrated circuit. Prototyping environment was used for two main purposes: as concept verification environment and as pre-silicon SW development environment. The first request was dictated by need to verify new IP blocks as much as close to real application, before concept freeze. Later was dictated by statement that long design cycle is no longer acceptable in the presence of shorter Time-to-Market pressures for products with increasingly shorter market windows.

Field Programmable Gate Array (FPGA) technology, powered with advanced simulation and synthesis tools is becoming the most preferred platform for the rapid prototyping of highly integrated digital systems – "System on a chip" (SoC) with multiple processors, audio, video peripheral blocks inside.



DTV chip architecture

The project deals with customization of ASIC RTL code (under development) for multi FPGA platform and as well as design of interface boards for connection of multi FPGA design to real world.

The initial prototyping concept was developed in a joint action with concept, HW and SW design engineers. A big ASIC design" was splitter into logical scenarios, capable to fit into chosen multi FPGA platform. For example there were separate video data flow scenarios, audio data flow scenario, communication peripherals scenarios, flash memories scenario, etc. Multi processor SW architecture and SW debugging tools were also adjusted to such logical scenarios.

The main challenges during development were:

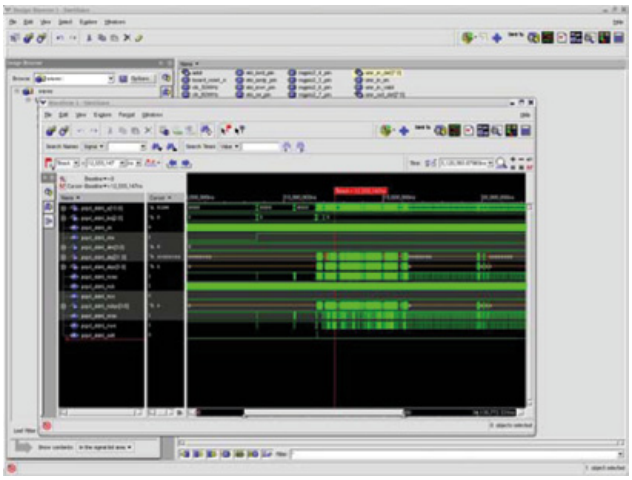
- Customization of ASIC RTL code while it is still under development
- Design of FPGA specific workarounds for ASIC specific RTL modules (memories, PLLs, pads, clocks, ...)
- Partitioning of design between multiple FPGA
- Designing platform extension boards
- Endeavor to do all previous listed and keep design as fast as possible, e.g. more close to ASIC speed

The project started several weeks after ASIC RTL design was kicked off and last all the way until 1st silicon was brought up on the evaluation board. Development in such "ever-changing ASIC RTL code" environment required great team flexibility and short turnover time between new ASIC RTL code release and FPGA RTL code release.

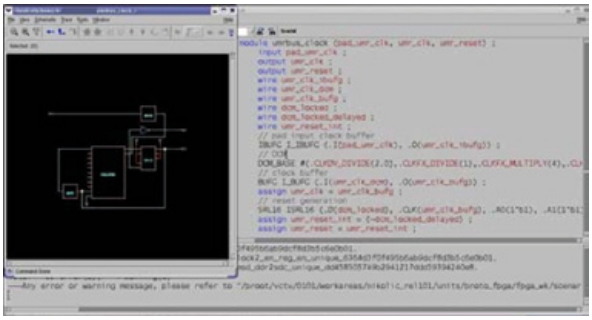
FPGA development process comprised of two major parts:

- Functional co-verification of ASIC and FPGA RTL codes.
- Synthesis of FPGA RTL code for specific prototyping platform

Functional co-verification was done using Cadence Incisive simulation SW and Novas Verdi code level debugger.



Screenshot of Cadence IUS SW GUI



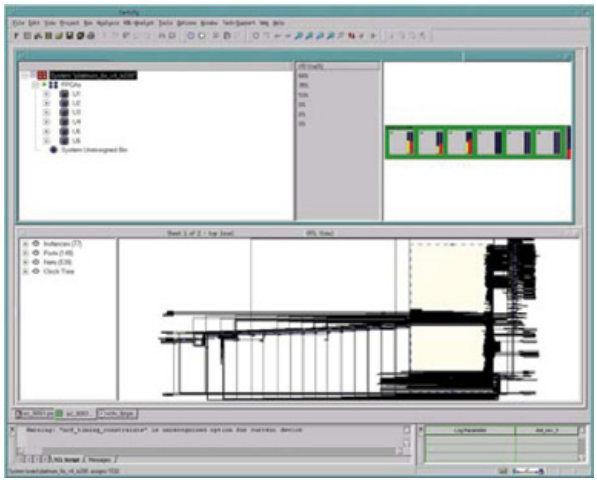
Screenshot of Novas Verdi SW GUI

Synthesis was performed with Synopsys Certify, ProDesign Chipit Manager and Xilinx XST SW, all for prototyping platform ProDesign CHIPit Platinum.

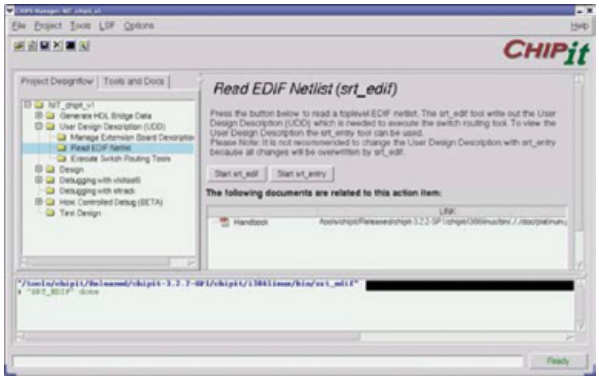
Photo of prototyping platform

The developed prototyping environment is able to provide "near ASIC" functionality, easy SW development/ debugging and RTL code debugging, through supported JTAG probes, as well as versatile interfaces. Interfaces on extension boards provide window from FPGA digital design into video, audio, communication and external memory world.

The development lasted half a year. It involved three FPGA design engineers, one hardware engineer for schematics and PCB design and one engineer for software support for FPGA design bring up, as well as one project manager.



Screenshot of Synopsys Certify SW GUI



Screenshot of ProDesign Chipit Manager SW GUI

Benefits

The project covered the complete development from the prototyping environment idea until HW/SW prototyping platform. All development steps were either conducted or organized by RT-RK, in correspondence with the customer. The final solution fulfills the customer

requirements in terms of performances. The complete development process and costs were transparent to the customer via regular meetings and appropriate reports.

Prototyping Environment Gallery

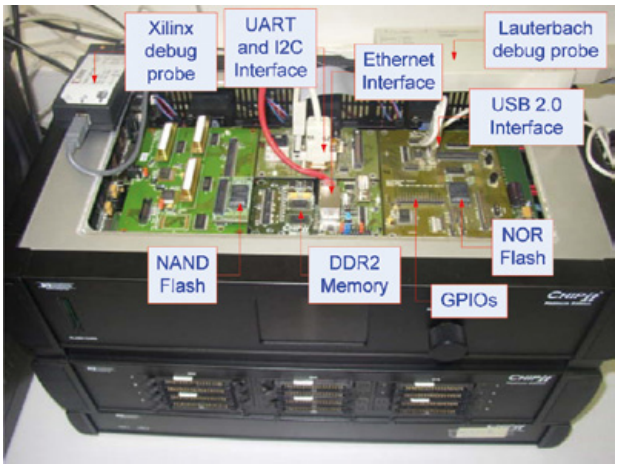


Photo of prototyping environment for communication peripherals and flash memories scenario

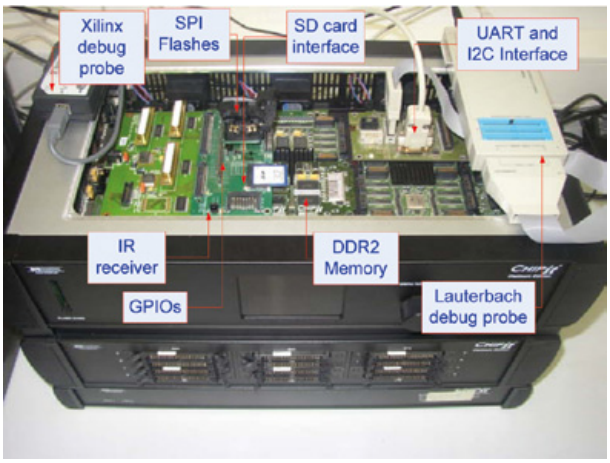


Photo of prototyping environment for video scenario

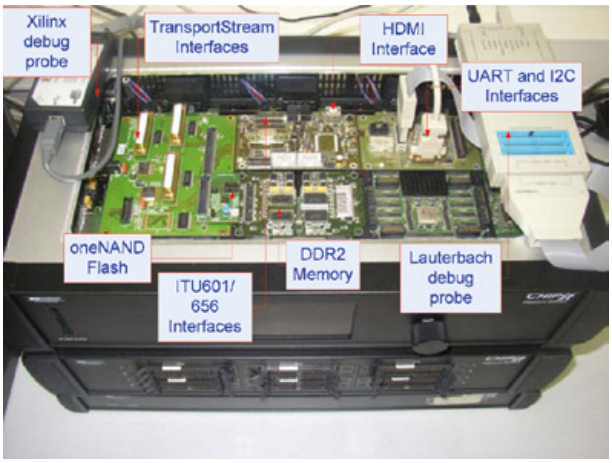


Photo of prototyping environment for lash memories and SD cards scenario

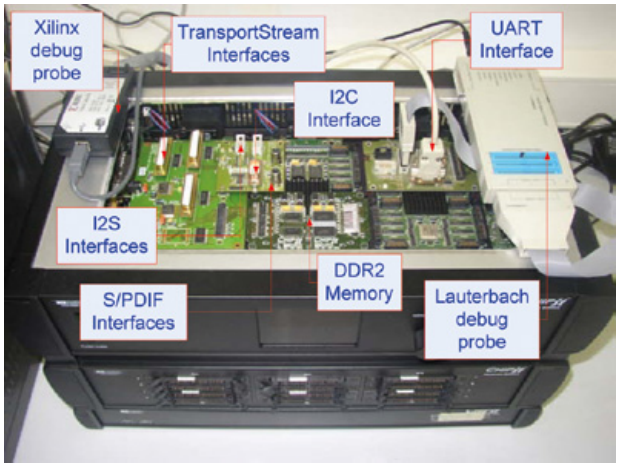


Photo of prototyping environment for audio scenario

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